Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **I0**
2. **N.O0**
3. **I1**
4. **N.O1**
5. **I2**
6. **N.O2**
7. **GND**
8. **N.O3**
9. **I3**
10. **N.O4**
11. **I4**
12. **N.O5**
13. **I5**
14. **VCC**

**DIE ID**

**2 1 14 13 12**

**5 6 7 8 9**

**11**

**10**

**3**

**4**

**25 mils**

**31 mils**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0029” X .0029”**

**Backside Potential: GND (can leave FLOATING)**

**Mask Ref: AC14W**

**APPROVED BY: DK DIE SIZE .025” X .031” DATE: 11/29/21**

**MFG: FAIRCHILD THICKNESS .014” P/N: 54AC14**

**DG 10.1.2**

#### Rev B, 7/19/02